

SANYO Semiconductors DATA SHEET



Monolithic Linear IC For the DVD Player Analog Video Signal I/F Driver

Overview

The LA7138M is a video output interface IC for DVD players. It is an ideal DVD player driver IC that generates analog video signals such as composite/S and component/RGB signals. Incorporating Y/C-MIX, the LA7138M can dispense with the composite output that would otherwise have to be provided by a DA converter.

Feature

- Video S/N ratio: -80dB.
- f characteristics: 10MHz flat.
- Y/C time difference: 2ns maximum.
- Signal dynamic range: 170 IRE.
- Supports all types of video signals including the composite/S, component, and base-band (RGB) signals; the internal input configuration is selected under microcontroller control (input capacitors to be used in common).
- Provides two channels of 75Ω driver outputs each of which can be muted on and off independently under microcontroller control.
- Internally generates clamp pulses that are necessary when receiving the component input signals.
- The amplifier gain is selectable from 8.5dB and 6dB.
- The on-chip regulator circuit provides stable DC voltages that are immune to V_{CC} fluctuations.

Function

- Clamp.
- Amplifier.
- 75 Ω driver.

- Y/C-MIX.
- DC voltage output for S1 and S2.

Specifications

Maximum Ratings at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V _{CC} max		15.0	V
Allowable power dissipation	Pdmax	Ta≤75°C, Mounted on a board*	525	mW
Operating temperature	Topr		-20 to +75	°C
Storage temperature	Tstg		-40 to +150	°C

*: As mounted to the glass epoxy made board of a size 114.3×76.1×1.6mm³

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Recommended Operating Conditions at $Ta = 25^{\circ}C$

Parameter	Symbol	Conditions	Ratings	Unit
Recommended supply voltage A	V _{CC} A	*	12.0	V
Operating supply voltage range A	V _{CC} op A		9.0 to 13.0	V
Recommended supply voltage B	V _{CC} B	*	8.0	V
Operating supply voltage range B	V _{CC} op B		7.5 to 8.5	V
Input pin voltage application range	V _{IN}	V _{CC} op A, B+0.3≤13V	-0.3 to V _{CC} op A, B+0.3	V

*: A different operation circuit is recommended for recommended supply voltages A and B. An external operation circuit with a PNP transistor for voltage drop is recommended for the recommended supply voltage A.

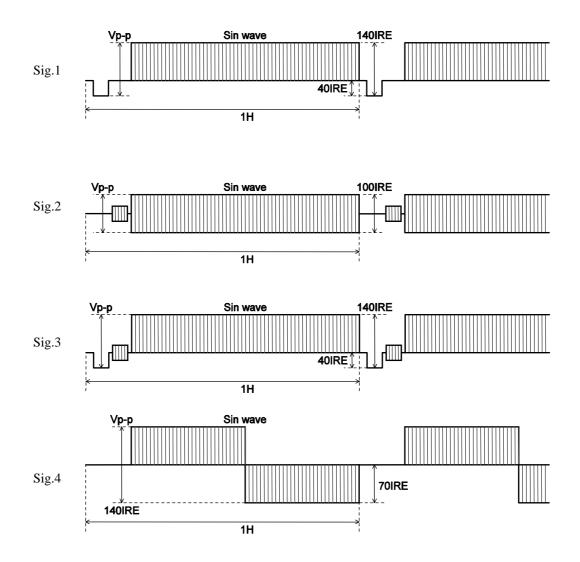
Electrical Characteristics at Ta = 25°C, $V_{CC}A = 9.0$ to 13.0V, $V_{CC}B = 7.5$ to 8.5V

Parameter	Symbol	Input	Test	Conditions		Ratings		Unit
T didineter	Cymbol	signal	point	Conditions	min	typ	max	011
Current drain (1)	ICC1		9pin	Current drain of VIDEO system.	29.6	37.0	44.4	mA
(A) Pin 10 (Y signal)	input when th	ne comp	osite/S is	s selected.				
AMP-GAIN (Low)	G _Y M	Sig.1	T13/15	GAIN when 996mVp-p, 100kHz is entered.	5.05	5.27	5.48	dB
AMP-GAIN (High)	G _Y H	Sig.1	T13/15	GAIN when 761mVp-p, 100kHz is entered.	7.38	7.6	7.81	dB
Clamp voltage	С ₁₀ Н	Sig.1	T10	Potential of sink chip of T10 when 761mVp-p is entered.	3.85	4.20	4.55	V
(B) Pin 6 (chroma si	gnal) input wh	en the c	composite	e/S is selected.				
AMP-GAIN (Low)	G _C M	Sig.2	T17/19	GAIN when 711mVp-p, 3.58MHz is entered.	5.05	5.27	5.48	dB
AMP-GAIN (High)	GCH	Sig.2	T17/19	GAIN when 544mVp-p, 3.58MHz is entered.	7.38	7.6	7.81	dB
Chroma input DC voltage	D ₆ H	Sig.2	Т6	Offset voltage of T6 when 544 mVp-p is entered.	4.4	4.75	5.1	V
(C) Pin 3 (composite	e signal) input	when th	e compo	site is selected.				
AMP-GAIN (Low)	G _S M1	Sig.3	T21/23	GAIN when 996mVp-p, 100kHz is entered.	5.05	5.27	5.48	dB
AMP-GAIN (High)	G _S H1	Sig.3	T21/23	GAIN when 761mVp-p, 100kHz is entered.	7.38	7.6	7.81	dE
Clamp voltage	C ₃ H	Sig.3	Т3	Potential of sink chip of T3 when 761mVp-p is entered.	4.0	4.35	4.7	V
(D) Pins 6, 10 (S sig	· · ·							
	· · ·			ed. with pin 2, (See the block diagram.) GAIN when 996mVp-p, 100kHz or 711mVp-p,	4.92	5.27	5.61	dB
To select "S", in	sert a 5.1kΩ ι	resistor i Sig.1 Sig.2 Sig.1	n series	with pin 2, (See the block diagram.) GAIN when 996mVp-p, 100kHz or 711mVp-p, 3.58MHz is entered. GAIN when 761mVp-p, 100kHz or 544mVp-p,	4.92 7.25	5.27 7.6	5.61	-
To select "S", in AMP-GAIN (Low) AMP-GAIN (High)	Sert a 5.1kΩ r G _S M2 G _S H2	Sig.1 Sig.2 Sig.1 Sig.1 Sig.2	n series T21/23 T21/23	with pin 2, (See the block diagram.) GAIN when 996mVp-p, 100kHz or 711mVp-p, 3.58MHz is entered. GAIN when 761mVp-p, 100kHz or 544mVp-p, 3.58MHz is entered.	_			-
To select "S", in AMP-GAIN (Low) AMP-GAIN (High) (E) GAIN ratio of sig	sert a 5.1kΩ i G _S M2 G _S H2 nals when the	resistor i Sig.1 Sig.2 Sig.1 Sig.2 e compos	n series T21/23 T21/23 site is se	with pin 2, (See the block diagram.) GAIN when 996mVp-p, 100kHz or 711mVp-p, 3.58MHz is entered. GAIN when 761mVp-p, 100kHz or 544mVp-p, 3.58MHz is entered. lected.	7.25	7.6	7.94	dE
To select "S", in AMP-GAIN (Low) AMP-GAIN (High) (E) GAIN ratio of sig Y/chroma	Sert a 5.1kΩ r G _S M2 G _S H2	esistor i Sig.1 Sig.2 Sig.1 Sig.2 composition Sig.1	n series T21/23 T21/23 site is se T13/15T	with pin 2, (See the block diagram.) GAIN when 996mVp-p, 100kHz or 711mVp-p, 3.58MHz is entered. GAIN when 761mVp-p, 100kHz or 544mVp-p, 3.58MHz is entered. lected.	_			dE
To select "S", in AMP-GAIN (Low) AMP-GAIN (High) (E) GAIN ratio of sig Y/chroma -AMP-GAIN ratio Y/composite-AMP-	sert a 5.1kΩ i G _S M2 G _S H2 nals when the	esistor i Sig.1 Sig.2 Sig.1 Sig.2 compose Sig.1 Sig.2 Sig.1	n series T21/23 T21/23 site is se T13/15T 17/19 T13/15	with pin 2, (See the block diagram.) GAIN when 996mVp-p, 100kHz or 711mVp-p, 3.58MHz is entered. GAIN when 761mVp-p, 100kHz or 544mVp-p, 3.58MHz is entered. lected.	7.25	7.6	7.94	dE %
To select "S", in AMP-GAIN (Low) AMP-GAIN (High) (E) GAIN ratio of sig Y/chroma -AMP-GAIN ratio Y/composite-AMP- GAIN ratio Chroma/composite	Sert a 5.1kΩ r G _S M2 G _S H2 nals when the ΔY _C	esistor i Sig.1 Sig.2 Sig.1 Sig.2 compose Sig.1 Sig.2 Sig.1 Sig.2 Sig.1 Sig.3 Sig.2	n series T21/23 T21/23 site is se T13/15T 17/19 T13/15 T21/23 T17/19	with pin 2, (See the block diagram.) GAIN when 996mVp-p, 100kHz or 711mVp-p, 3.58MHz is entered. GAIN when 761mVp-p, 100kHz or 544mVp-p, 3.58MHz is entered. lected. GAIN ratio between G _Y H of (A) and G _C H of (B).	-3	7.6	7.94	dB %
To select "S", in AMP-GAIN (Low) AMP-GAIN (High) (E) GAIN ratio of sig Y/chroma -AMP-GAIN ratio Y/composite-AMP- GAIN ratio Chroma/composite -AMP-GAIN ratio	$\begin{array}{c c} \text{sert a } 5.1 \text{k}\Omega \text{ I} \\ \hline \text{G}_{S}\text{M2} \\ \hline \text{G}_{S}\text{H2} \\ \hline \text{nals when the} \\ \hline \Delta^{Y}\text{C} \\ \hline \Delta^{Y}\text{C} \\ \hline \Delta^{Y}\text{S1} \\ \hline \Delta C\text{S1} \end{array}$	esistor i Sig.1 Sig.2 Sig.1 Sig.2 compose compose Sig.1 Sig.2 Sig.1 Sig.2 Sig.3	n series T21/23 T21/23 site is se T13/15T 17/19 T13/15 T21/23 T17/19 T21/23	with pin 2, (See the block diagram.) GAIN when 996mVp-p, 100kHz or 711mVp-p, 3.58MHz is entered. GAIN when 761mVp-p, 100kHz or 544mVp-p, 3.58MHz is entered. lected. GAIN ratio between G _Y H of (A) and G _C H of (B). GAIN ratio between G _Y H of (A) and G _S H1 of (C). GAIN ratio between G _C H of (B) and G _S H1 of (C).	-3	0	7.94	dB dB % %
To select "S", in AMP-GAIN (Low) AMP-GAIN (High) (E) GAIN ratio of sig Y/chroma -AMP-GAIN ratio Y/composite-AMP- GAIN ratio Chroma/composite -AMP-GAIN ratio (F) GAIN ratio of sig	$\begin{array}{c c} \text{sert a } 5.1 \text{k}\Omega \text{ I} \\ \hline \text{G}_{S}\text{M2} \\ \hline \text{G}_{S}\text{H2} \\ \hline \text{nals when the} \\ \hline \Delta^{Y}\text{C} \\ \hline \Delta^{Y}\text{C} \\ \hline \Delta^{Y}\text{S1} \\ \hline \Delta C\text{S1} \end{array}$	esistor i Sig.1 Sig.2 Sig.1 Sig.2 comport Sig.1 Sig.2 Sig.1 Sig.3 Sig.2 Sig.3 Sig.2 Sig.3 Sig.2 Sig.3 Sig.1	n series T21/23 T21/23 site is se T13/15T 17/19 T13/15 T21/23 T17/19 T21/23 al is selec T13/15	with pin 2, (See the block diagram.) GAIN when 996mVp-p, 100kHz or 711mVp-p, 3.58MHz is entered. GAIN when 761mVp-p, 100kHz or 544mVp-p, 3.58MHz is entered. lected. GAIN ratio between G _Y H of (A) and G _C H of (B). GAIN ratio between G _Y H of (A) and G _S H1 of (C). GAIN ratio between G _C H of (B) and G _S H1 of (C).	-3	0	7.94	dE %
To select "S", in AMP-GAIN (Low) AMP-GAIN (High) (E) GAIN ratio of sig Y/chroma -AMP-GAIN ratio Y/composite-AMP- GAIN ratio Chroma/composite -AMP-GAIN ratio (F) GAIN ratio of sig Y/S-AMP-GAIN ratio	$\begin{tabular}{ c c c c c c c } \hline Sert a 5.1 k\Omega t \\ \hline G_S M2 \\ \hline G_S H2 \\ \hline als when the \\ \hline \Delta Y_C \\ \hline \Delta Y_S 1 \\ \hline \Delta C_S 1 \\ \hline als when the \\ \hline \end{tabular}$	esistor i Sig.1 Sig.2 Sig.1 Sig.2 comport Sig.1 Sig.2 Sig.1 Sig.2 Sig.3 Sig.2 Sig.3 Sig.2 Sig.3	n series T21/23 T21/23 site is se T13/15T 17/19 T13/15 T21/23 T17/19 T21/23 al is selec	with pin 2, (See the block diagram.) GAIN when 996mVp-p, 100kHz or 711mVp-p, 3.58MHz is entered. GAIN when 761mVp-p, 100kHz or 544mVp-p, 3.58MHz is entered. lected. GAIN ratio between G _Y H of (A) and G _C H of (B). GAIN ratio between G _Y H of (A) and G _S H1 of (C). GAIN ratio between G _C H of (B) and G _S H1 of (C). cted.	-3 -3 -3	7.6 0 0 0	7.94	dE %
To select "S", in AMP-GAIN (Low) AMP-GAIN (High) (E) GAIN ratio of sig Y/chroma -AMP-GAIN ratio Y/composite-AMP- GAIN ratio Chroma/composite -AMP-GAIN ratio (F) GAIN ratio of sig Y/S-AMP-GAIN ratio Chroma/S-AMP-	$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	esistor i Sig.1 Sig.2 Sig.1 Sig.2 compose Sig.1 Sig.2 Sig.1 Sig.2 Sig.3 Sig.2 Sig.3 Sig.2 Sig.1 Sig.2 Sig.1 Sig.2 Sig.1 Sig.2 Sig.1	n series T21/23 T21/23 site is se T13/15T 17/19 T13/15 T21/23 T17/19 T21/23 T13/15 T21/23 T17/19 T21/23	with pin 2, (See the block diagram.) GAIN when 996mVp-p, 100kHz or 711mVp-p, 3.58MHz is entered. GAIN when 761mVp-p, 100kHz or 544mVp-p, 3.58MHz is entered. lected. GAIN ratio between G _Y H of (A) and G _C H of (B). GAIN ratio between G _Y H of (A) and G _S H1 of (C). GAIN ratio between G _C H of (B) and G _S H1 of (C). cted. GAIN ratio between G _Y H of (A) and G _S H2 of (D) GAIN ratio between G _C H of (B) and G _S H2 of (D).	-3 -3 -3 -4.5	7.6 0 0 0	7.94 3 3 3 4.5	dE % %
To select "S", in AMP-GAIN (Low) AMP-GAIN (High) (E) GAIN ratio of sig Y/chroma -AMP-GAIN ratio Y/composite-AMP- GAIN ratio Chroma/composite -AMP-GAIN ratio (F) GAIN ratio of sig Y/S-AMP-GAIN ratio Chroma/S-AMP- GAIN ratio (G) Pin 10 (Y signal)	$\begin{tabular}{ c c c c c c c c c c c c c c c c c c c$	esistor i Sig.1 Sig.2 Sig.1 Sig.2 compose Sig.1 Sig.2 Sig.1 Sig.2 Sig.3 Sig.2 Sig.3 Sig.2 Sig.1 Sig.2 Sig.1 Sig.2 Sig.1 Sig.2 Sig.1	n series T21/23 T21/23 site is se T13/15T 17/19 T13/15 T21/23 T17/19 T21/23 T13/15 T21/23 T17/19 T21/23	with pin 2, (See the block diagram.) GAIN when 996mVp-p, 100kHz or 711mVp-p, 3.58MHz is entered. GAIN when 761mVp-p, 100kHz or 544mVp-p, 3.58MHz is entered. lected. GAIN ratio between G _Y H of (A) and G _C H of (B). GAIN ratio between G _Y H of (A) and G _S H1 of (C). GAIN ratio between G _C H of (B) and G _S H1 of (C). cted. GAIN ratio between G _Y H of (A) and G _S H2 of (D) GAIN ratio between G _C H of (B) and G _S H2 of (D).	-3 -3 -3 -4.5	7.6 0 0 0	7.94 3 3 3 4.5	dE %
To select "S", in AMP-GAIN (Low) AMP-GAIN (High) (E) GAIN ratio of sig Y/chroma -AMP-GAIN ratio Y/composite-AMP- GAIN ratio Chroma/composite -AMP-GAIN ratio (F) GAIN ratio of sig Y/S-AMP-GAIN ratio Chroma/S-AMP- GAIN ratio	$\begin{array}{c c} \text{sert a } 5.1 \text{k}\Omega \text{ I} \\ \hline \text{G}_{S}\text{M2} \\ \hline \text{G}_{S}\text{H2} \\ \hline \text{nals when the} \\ \hline \Delta \text{Y}_{C} \\ \hline \Delta \text{Y}_{S}1 \\ \hline \Delta \text{C}_{S}1 \\ \hline \text{nals when the} \\ \hline \Delta \text{Y}_{S}2 \\ \hline \Delta \text{C}_{S}2 \\ \hline \text{nals when the} \\ \hline \end{array}$	esistor i Sig.1 Sig.2 Sig.1 Sig.2 Compose Sig.1 Sig.2 Sig.1 Sig.2 Sig.1 Sig.2 Sig.3 Sig.2 Sig.3 Sig.2 Sig.1 Sig.2 Sig.1 Sig.2 Sig.1 Sig.2 ne compo	n series T21/23 T21/23 site is se T13/15T T7/19 T13/15 T21/23 T17/19 T21/23 T13/15 T21/23 T17/19 T21/23 Onent is	with pin 2, (See the block diagram.) GAIN when 996mVp-p, 100kHz or 711mVp-p, 3.58MHz is entered. GAIN when 761mVp-p, 100kHz or 544mVp-p, 3.58MHz is entered. lected. GAIN ratio between G _Y H of (A) and G _C H of (B). GAIN ratio between G _Y H of (A) and G _S H1 of (C). GAIN ratio between G _C H of (B) and G _S H1 of (C). cted. GAIN ratio between G _Y H of (A) and G _S H2 of (D) GAIN ratio between G _C H of (B) and G _S H2 of (D). selected.	-3 -3 -3 -3 -3 -4.5 -4.5	7.6 0 0 0 0	7.94 3 3 3 4.5 4.5	dE % %

Parameter	Symbol	Input	Test	Conditions		Ratings		Uni
i didilotor	Cymbol	signal	point		min	typ	max	011
(H) Pin 6 (B-Y or R-)	r signal) wher	n the cor	mponent	is selected.				1
AMP-GAIN (Low)	G _N M	Sig.4	T17/19	GAIN when 996mVp-p, 100 kHz is entered.	5.05	5.27	5.48	dE
AMP-GAIN (High)	G _N H	Sig.4	T17/19	GAIN when 761mVp-p, 100 kHz is entered.	7.38	7.6	7.81	dE
Input pedestal clamp voltage	P ₆ H	Sig.4	Т6	Potential of pedestal of T6 when 761mVp-p is entered.	4.4	4.75	5.1	V
AMP-GAIN (Low)	G _N M	Sig.4	T21/23	GAIN when 996mVp-p, 100 kHz is entered.	5.05	5.27	5.48	dE
(I) Pin 3 (B-Y or R- Y	' signal) input	when th	ie compo	onent is selected.				
AMP-GAIN (High)	G _N H	Sig.4	T21/23	GAIN when 761mVp-p, 100 kHz is selected.	7.38	7.6	7.81	dE
Input pedestal clamp voltage	P ₃ H	Sig.4	Т3	Potential of pedestal of T3 when 761mVp-p is entered.	4.4	4.75	5.1	V
(J) GAIN ratio of sigr	hals when the	compor	nent is se	elected.				
Y/composite-AMP- GAIN ratio (1)	ΔΥ1	Sig.1 Sig.4	T13/15 T17/19	GAIN ratio between GYH of (E) and GNH of (F)	-3	0	3	%
Y/composite-AMP- GAIN ratio (2)	Δ Y2	Sig.1 Sig.4	T13/15 T21/23	GAIN ratio between G_YH of (E) and G_NH of (G)	-3	0	3	%
Component-AMP- GAIN ratio	ΔΝ	Sig.4 Sig.4	T17/19 T21/23	GAIN ratio between $G_{\ensuremath{N}}H$ of (F) and that of (G)	-3	0	3	%
(K) Pin 10 (RGB sigr	nal) input whe	-		is selected.				
AMP-GAIN (Low)	G _B M	Sig.1	T13/15	GAIN when 996mVp-p, 100 kHz is entered.	5.05	5.27	5.48	dE
AMP-GAIN (High)	G _B H	Sig.1	T13/15	GAIN when 761mVp-p, 100 kHz is entered.	7.38	7.6	7.81	dE
Input clamp voltage	с ₁₀ н	Sig.1 T10 Potential of sink chip of T10 when 761mVp-p is entered.		3.85	4.20	4.55	V	
(L) Pin 6 (RGB signa	al) Input when	the bas	e band is					
AMP-GAIN (Low)	G _B M	Sig.1	T13/15	GAIN when 996mVp-p, 100 kHz is entered.	5.05	5.27	5.48	dE
AMP-GAIN (High)	G _B H	Sig.1	T13/15	GAIN when 761mVp-p, 100 kHz is entered.	7.38	7.6	7.81	dE
Input clamp voltage	С ₆ Н	Sig.1	T10	Potential of sink chip of T10 when 761mVp-p is entered.	4.0	4.35	4.7	V
(M) Pin 3 (RGB sign	al) Input wher	n the bas	se band i					
AMP-GAIN (Low)	G _B M	Sig.1	T13/15	GAIN when 996mVp-p, 100 kHz is entered.	5.05	5.27	5.48	dE
AMP-GAIN (High)	G _B H	Sig.1	T13/15	GAIN when 761mVp-p, 100 kHz is entered.	7.38	7.6	7.81	dE
Input clamp voltage	С ₃ Н	Sig.1	T10	Potential of sink chip of T10 when 761mVp-p is entered.	4.0	4.35	4.7	V
(N) GAIN ratio of sig	nals when the	e base b	and is se					
Base bank –AMP- GAIN ratio (1)	ΔB1	Sig.1 Sig.1	T13/15 T17/19	GAIN ratio between G_BH of (I) and that of (J)	-3	0	3	%
Base band –AMP- GAIN ratio (2)	Δ B 2	Sig.1 Sig.1 Sig.1	T13/15 T21/23	GAIN ratio between G_BH of (I) and that of (K)	-3	0	3	%
Base band –AMP- GAIN ratio	Δ B 3	Sig.1 Sig.1 Sig.1	T17/19 T21/23	GAIN ratio between $G_{\mbox{\scriptsize B}}\mbox{\scriptsize H}$ of (J) and that of (K)	-3	0	3	%
	of GAIN (com	-		s and input signals, however, except for Y/C-N	IIX).			L
LPF 6MHz attenuation	F _Y 6	Sig.1	T13/15	Difference between GAIN and GγH when 761mVp-p, 6MHz is entered.	-0.5	0	+0.5	dE
LPF 10MHz attenuation	F _Y 10	Sig.1	T13/15	Difference between GAIN and GyH when 761mVp-p, 10MHz is entered.	-0.5	0	+0.5	dE
(P) DC voltage for or	utput mute (co	ommon t	o all mo					L
Pin 13 voltage	V ₁₃		T13	·	3.7	4.05	4.4	V
Pin 15 voltage	V13 V15		T15		3.7	4.05	4.4	v
Pin 17 voltage	V15 V17		T17		3.9	4.05	4.4	v
Pin 19 voltage			T19		3.9	4.25	4.6	v
i ii i ə voltaye	V ₁₉ V ₂₁		T21		3.9	4.25	4.6	V
Pin 21 voltage								/

Continued from preceding	page.							
Parameter	Symbol	Input	Test	Conditions		Ratings		Unit
Falameter	Symbol	signal	point	Conditions	min	typ	max	Unit
* Output DC voltage	e characteristic	s at Ta	= 25°C, '	V _{CC} A = 9.0 to 13.0V				
Output DC for 4: 3	V ₄₃		T16	For 4:3 mode control (no load)	0	0.01	0.35	V
Output DC for	V _{LB}		T16	For the Letter-Box mode control	2.05	2.2	2.35	V
Letter -Box				(Load current 500µA to flow out)				
Output DC for	V _{SQ}		T16	For squeeze mode control	4.4	4.7	5.0	V
squeeze				(Load current 500µA to flow out)				
* Output DC voltage	e characteristic	s at Ta⊧	= 25°C, '	V _{CC} B = 7.5 to 8.5V				
Output DC for 4: 3	V ₄₃		T16	For 4:3 mode control (no load)	0	0.01	0.35	V
Output DC for	V _{LB}		T16	For the Letter-Box mode control	1.90	2.15	2.40	V
Letter-Box				(Load current 500µA to flow out)				
Output DC for	V _{SQ}		T16	For squeeze mode control	4.15	4.60	5.00	V
squeeze				(Load current 500µA to flow out)				

Note) Each of AMP-GAIN and AMP-GAIN ratios is the value when the output pin part shown in the test circuit diagram is inserted.



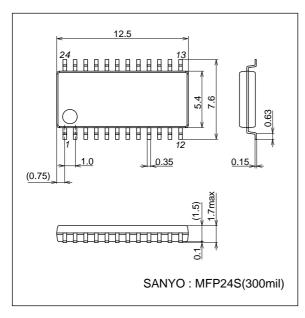
LA7138M

Parameter	Symbol	Conditions	Ratings				
Parameter	Symbol	Conditions	min	typ	max	Unit	
Except for Y/C-MIX	$(V_{CC}A = 9.0)$	to 13.0V, V _{CC} B = 7.5 to 8.5V)					
Channel crosstalk	СТ	The signal which becomes $1Vp-p$ at $f = 4MHz$ and with the output in		-65	-60	dB	
		C connection is entered in other channels. Measure the magnitude					
		of monitor channel output pins at 4MHz and specify the ratings as a					
		ratio relative to the magnitude of output pin of other channels at					
		4MHz.					
Video S/N ratio	SN	Enter the Y signal with 100% white and apply 3.3V to pin 11.		-80	-78	dB	
		Measure S/N of the output signal.					
		* Refer to Note 1.					
Differential gain	DG	Enter the 1Vp-p standard stair step signal (color) to obtain pin 11 =		0.5	2	%	
		OPEN. Measure the differential gain of the output signal, with the					
		output pin part shown in the measuring circuit diagram inserted.					
Differential phase	DP	Enter the 1Vp-p standard stair step signal (color) to obtain pin 11 =	-1	0	1	dB	
		OPEN. Measure the differential phase of the output signal, with the					
		output pin part shown in the measuring circuit diagram inserted.					
For Y/C-MIX (V _{CC} I	B = 7.5 to 8.5V)					
Channel crosstalk	СТ	The signal which becomes 1Vp-p at f = 4MHz and with the output in		-65	-60	dB	
		C connection is entered in other channels. Measure the magnitude					
		of monitor channel output pins at 4MHz and specify the ratings as a					
		ratio relative to the magnitude of output pin of other channels at					
		4MHz.					
Video S/N ratio	SN	Enter the Y signal with 100% white and add pin 11 = 3.3V. Measure		-74	-72	dB	
		S/N of the output signal.					
		* Refer to Note 1.					
Differential gain	DG	Enter the 761mVp-p standard stair step signal (color) to obtain pin		4	5.5	%	
		11 = 3.3V. Measure the differential gain of the output signal, with the					
		output pin part shown in the measuring circuit diagram inserted.					
Differential phase	DP	Enter the 761mVp-p standard stair step signal (color) to obtain pin	-1	0.5	1.5	dE	
		11 = 3.3V. Measure the differential phase of the output signal, with					
		the output pin part shown in the measuring circuit diagram inserted.					

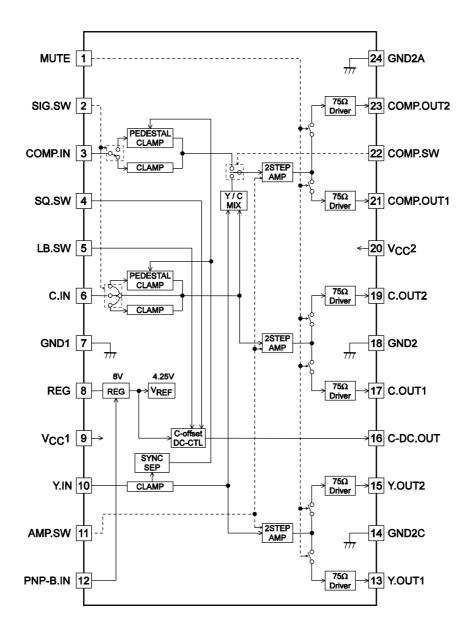
* Note 1) Since the noise in IC is dependent on the stability of regulator, it is recommended to connect a 470µF capacitor when the S/N ratio of -80dB is to be secured for controls other than Y/C-MIX. To secure the S/N ratio of -74dB for Y/C-MIX, set the supply voltage to 8V (V_{CC}B) and apply 8V also to this pin. (See the test circuit B.)

Package Dimensions

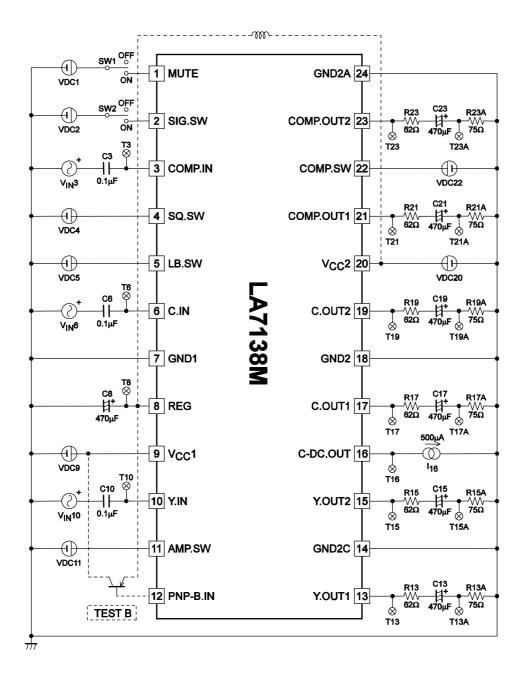
unit : mm 3112B



Block Diagram



Test Circuit



Input/Output form Diagram

	au Output R	1				
Pin No.	Pin name	I/O	Pin voltage	Input/ Output impedance	Function	Equivalent circuit
1	MUTE	I	1.7V	21kΩ	Mute control pin for video signal outputs (Pins 13, 15, 17, 19 and 21). Control can be made with a microcontroller operating on 3.3 to 5.0V power supply.	4.25V 8V ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓
2	SIG.SW	I	1.7V	21kΩ	Pin to select the input form of pins 3 and 6 according to the type of input signal (composite/s/component/ base band). Control can be made with a microcontroller operating on 3.3 to 5.0V power supply. Add a $5.1 k\Omega$ resistor in series externally.	
3	COMP.IN	1	4.5V	Clamp form	Video signal input pin. Enter the composite signal for input of the composite/S signal. Enter the B-Y or R-Y signal for input of the component signal. For input of the base band, enter any of RGB signals that have a sync signal. (This pin is connected to GND when the S signal is entered.)	
4	SQ.SW	1	2.4V	9.0GΩ	Pin to enter the squeeze information. Control can be made with a microcontroller that operates on 3.3 to 5.0V power supply.	
5	LB.SW	1	2.43V	8.1GΩ	Pin to enter the Letter-Box information. Control can be made with a microcontroller that operates on 3.3 to 5.0V power supply.	
22	COMP.SW	1	2.4V	9.0GΩ	Y/C-MIX ON/OFF control pin. Be sure to set this pin HIGH in cases other than composite/S control of pin 2. Control is possible with a microcontroller operating on 3.3 to 5.0V power supply or through selection of V _{CC} /GND on the substrate.	

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Continu	ued from preceding pag	ge.				
Pin No.	Pin name	1/0	Pin voltage	Input/ Output impedance	Function	Equivalent circuit
6	C.IN	1	4.8V	10κΩ	Video signal input pin. Enter the chroma signal for input of composite/S signal. Enter the B-Y or R-Y signal for input of the component signal input. For input of the base band signal, enter any of RGB signals that have a sync signal.	100μ 100μ
8	REG	0	8V	1.5kΩ	Pin for the regulator that generates an 8V supply voltage in IC. To use the supply voltage of 12V, connect a collector of the external PNP transistor (see the test circuit A). Since the noise in IC is dependent on the stability of regulator, it is recommended to connect a 470 μ F capacitor when the S/N ratio of –80dB is to be secured for controls other than Y/C-MIX. To secure the S/N ratio of –74dB for Y/C-MIX, set the supply voltage to 8V (V _{CC} B) and apply 8V also to this pin. (See the test circuit B.)	12kG 29.2kG 12kG 29.2kG 12kG 29.2kG 10kG 15kG 10kG 15kG 10kG 15kG 10kG 15kG 10kG 15kG 10bF 0
10	Y.IN	I	4.2V	Clamp form	Video signal input pin. Enter the Y signal for input of composite/S and component signal. For input of the base band signal, enter any of RGB signals that have a sync signal.	N 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
11	AMP.SW	I	2.4V	9.0GΩ	Control pin to select the AMP gain according to the input signal amplitude. Control is possible with a microcontroller that operates on 3.3 to 5.0V power supply as well as through selection of V_{CC} /GND on a substrate.	
12	PNP-B-IN	0	3.4V	4.0GΩ	Base input pin of the external PNP transistor for the 8V regulator. Connect to the transistor in case of the supply voltage of 12V (see the test circuit A). To use the supply voltage of 8V, keep this pin open (see the test circuit B).	

Pin No.	Pin name	I/O	Pin voltage	Input/ Output impedance	Function	Equivalent circuit
13	Y.OUT1	0	2.7V	11.6Ω	Video signal output pin. Drives the video signal entered in pin 10 by	8V 8V ↑ ↑
15	Y.OUT2	0	2.7V	11.6Ω	75Ω. Mute possible with pin 1.	L COS
17	C.OUT1	0	3.9V	11.6Ω	Video signal output pin. Drives the video signal entered in pin 6 by 75Ω .	-K A
19	C.OUT2	0	3.9V	11.6Ω	Mute possible with pin 1.	
21	COMP.OUT1	0	3.57V	11.6Ω	Video signal output pin. Drives the video signal entered in pin 3 by 75Ω .	
23	COMP.OUT2	0	3.57V	11.6Ω	Mute possible with pin 1.	m m m
16	C-DC.OUT	0	4.7V	4.1Ω	S1/S2 DC voltage output pin. Outputs 0V for the 4: 3 mode, 2.2V for the Letter-Box mode, and 5V for the squeeze mode. Connect with a $10k\Omega$ resistor after capacitive coupling of chroma signal output.	
9	V _{CC} 1	P	12V OR 8.0V		V_{CC} for a signal processing circuit. To use the supply voltage of 12V, connect an emitter of external PNP transistor (see the test circuit A). Insert a capacitor of around 47µF between this V_{CC} and pin 7.	
20	V _{CC} 2	Ρ	8V		V_{CC} for the 75 Ω drive circuit. Insert a capacitor of around 47 μ F between this V_{CC} and GND of the 75 Ω drive circuit. Pay due attention to the layout because the output signal has a substantial amplitude.	
7	GND1	Р	0V		GND for the signal processing circuit.	
14	GND2	Р	0V		GND of the 75Ω drive circuit (pins 13 and 15). Pay due attention on the layout because the output signal has a substantial amplitude.	
18	GND2B	Р	0V		GND of the 75Ω drive circuit (pins 17 and 19). Pay due attention to the layout because the output signal has a substantial amplitude.	
24	GND2A	Р	0V		GND of the 75 Ω drive circuit (pins 21 and 23). Pay due attention on the layout because the output signal has a substantial amplitude.	

Control Pin Function Table

Pin No.	Pin condition	LOW	OPE	N	HIGH	
	Pin voltage	0 to 0.6V	1.55 to 1.75V		2.7 to 5V	
Pin 1	Mute of 75Ω driver	13,17,21 mute	No m	ute	15,19,23 mute	
Pin 2	Pin voltage	0 to 0.6V	1.55 to 1.75V		2.7 to 5V	
(Y point)	Signal input mode select	Composite/S	Base band		Component	
Pin 11	Pin voltage	0 to 1V		2.7 to 8V (Note)		
PIN 11	AMP-GAIN select	6dB		8.5dB		
	Pin voltage	0 to 1V	0 to 1V		2.7 to 8V (Note)	
Pin 22	Y/C-MIX Control	Y/C-MIX		Composite		

Note: Do not apply to pins 11 and 22 a voltage higher than the REG & V_{CC}2 voltages of pins 8 and 20.

* Do not use Y/C-MIX for cases other than composite/S.

* For composite, the chroma signal is entered with pin 6 in C connection, the composite signal is entered with pin 3 clamped, and the Y signal is entered with pin 9 clamped. However, for S, Pin 3 has no input.

For component, the B-Y/R-Y signal is entered with pins 3 and 6 clamped to pedestal and the Y signal is entered with pin 10 clamped.

For base band, the RGB signal is entered with pins 3, 6, and 10 clamped.

Do not use Pins 11 and 22 in the OPEN state.

Pin 4	Pin 5	Pin 16 output DC
0 to 1V	0 to 1V	LOW (0V) \rightarrow 4:3Mode
0 to 1V	2.6 to 5V	MIDDLE (2.5V) \rightarrow Letter-Box mode
2.6 to 5V	0 to 1V	HIGH (5V) \rightarrow Squeeze mode
2.6 to 5V	2.6 to 5V	Not allowed

Switch condit	lions						ſ	
Symbol		1	Control volta		1	1	Switch co	onditions
	VDC1	VDC2	VDC4	VDC5	VDC11	VDC22	SW1	SW2
I _{CC} 1	0	0	3.3	0	3.3	3.3	ON	ON
I _{CC} 2	0	0	3.3	0	3.3	3.3	ON	ON
(A) Pin 10 (Y signal)	input when t	he composite	/S is selected	•	1	•		
G _Y M	0/3.3	0	*	*	0	3.3	ON/OFF	ON
G _Y H	0/3.3	0	*	*	3.3	3.3	ON/OFF	ON
С ₁₀ Н	0/3.3	0	*	*	3.3	3.3	ON/OFF	ON
(B) Pin 6 (chorma si	gnal) input wi	nen the comp	osite/S is sele	ected.				
G _C M	0/3.3	0	*	*	0	3.3	ON/OFF	ON
G _С Н	0/3.3	0	*	*	3.3	3.3	ON/OFF	ON
С ₆ Н	0/3.3	0	*	*	3.3	3.3	ON/OFF	ON
(C) Pin 3 (composite	e signal) input	when the co	mposite is sel	ected.	1	•		
G _S M1	0/3.3	0	*	*	0	3.3	ON/OFF	ON
G _S H1	0/3.3	0	*	*	3.3	3.3	ON/OFF	ON
С ₃ Н	0/3.3	0	*	*	3.3	3.3	ON/OFF	ON
(D) GAIN ratio of sig	nals when th	e composite/S	S is selected.			•		
G _S M2	0/3.3	0	*	*	0	0	ON/OFF	ON
G _S H2	0/3.3	0	*	*	3.3	0	ON/OFF	ON
(E) GAIN ratio of sig	nals when the	e composite i	s selected.					
ΔY_C	0/3.3	0	*	*	3.3	3.3	ON/OFF	ON
∆Y _S 1	0/3.3	0	*	*	3.3	3.3	ON/OFF	ON
$\Delta C_{S}1$	0/3.3	0	*	*	3.3	3.3	ON/OFF	ON
(F) GAIN ratio of sig	nals when the	e S is selecte	d.					
ΔY _S 2	0/3.3	0	*	*	3.3	0	ON/OFF	ON
∆C _S 2	0/3.3	0	*	*	3.3	0	ON/OFF	ON
(G) Pin 10 (Y signal) input when t	he componer	nt is selected.					
G _Y M	0/3.3	3.3	*	*	0	3.3	ON/OFF	ON
G _Y H	0/3.3	3.3	*	*	3.3	3.3	ON/OFF	ON
С ₁₀ Н	0/3.3	3.3	*	*	3.3	3.3	ON/OFF	ON
(H) Pin 6 (B-Y or R-	Y signal) inpu	t when the co	mponent is s	elected.				
G _N М	0/3.3	3.3	*	*	0	3.3	ON/OFF	ON
G _N H	0/3.3	3.3	*	*	3.3	3.3	ON/OFF	ON
P ₆ H	0/3.3	3.3	*	*	3.3	3.3	ON/OFF	ON
(I) Pin 3 (B-Y or R-Y	' signal) input	when the cor	nponent is se	lected.				
G _N М	0/3.3	3.3	*	*	0	3.3	ON/OFF	ON
G _N H	0/3.3	3.3	*	*	3.3	3.3	ON/OFF	ON
P ₃ H	0/3.3	3.3	*	*	3.3	3.3	ON/OFF	ON
(J) GAIN ratio of sig	nals when the	e component	is selected.					
ΔΥ1	0/3.3	3.3	*	*	3.3	3.3	ON/OFF	ON
ΔΥ2	0/3.3	3.3	*	*	3.3	3.3	ON/OFF	ON
ΔN	0/3.3	3.3	*	*	3.3	3.3	ON/OFF	ON
(K) Pin 10 (RGB signal) input when the	e base band is	selected.	-		•		
G _B M	0/3.3	*	*	*	0	3.3	ON/OFF	OFF
G _B H	0/3.3	*	*	*	3.3	3.3	ON/OFF	OFF
с ₁₀ н	0/3.3	*	*	*	3.3	3.3	ON/OFF	OFF
(L) Pin 6 (RGB signal)	input when the	base band is se	elected.					
G _B M	0/3.3	*	*	*	0	3.3	ON/OFF	OFF
G _B H	0/3.3	*	*	*	3.3	3.3	ON/OFF	OFF
с ₆ н	0/3.3	*	*	*	3.3	3.3	ON/OFF	OFF
(M) Pin 3 (RGB signal)		base band is s	elected.	L	1	I		L
, , , , , , , , , , , , , , , , , , , ,	0/3.3	*	*	*	0	3.3	ON/OFF	OFF
GeM	0/3.3							
G _B M G _B H	0/3.3	*	*	*	3.3	3.3	ON/OFF	OFF

*: Any condition

Symbol	Control voltage (Unit: V)						Switch conditions	
	VDC1	VDC2	VDC4	VDC5	VDC11	VDC22	SW1	SW2
N) GAIN ratio of sig	nals when the bas	e band is selec	ted					
Δ B 1	0/3.3	*	*	*	3.3	3.3	ON/OFF	OFF
$\Delta B2$	0/3.3	*	*	*	3.3	3.3	ON/OFF	OFF
$\Delta B3$	0/3.3	*	*	*	3.3	3.3	ON/OFF	OFF
(O) f characteristics	of GAIN (common	to all modes a	nd input signals	s, however, exc	cept for Y/C-MI	X)		
F _Y 6	0/3.3	0	*	*	3.3	3.3	ON/OFF	ON
F _Y 10	0/3.3	0	*	*	3.3	3.3	ON/OFF	ON
(P) DC voltage for o	utput mute (comm	on to all modes	5)					
V ₁₃	0	*	*	*	0/3.3	0/3.3	ON	*
V ₁₅	3.3	*	*	*	0/3.3	0/3.3	ON	*
V ₁₇	0	*	*	*	0/3.3	0/3.3	ON	*
V ₁₉	3.3	*	*	*	0/3.3	0/3.3	ON	*
V ₂₁	0	*	*	*	0/3.3	0/3.3	ON	*
V ₂₃	3.3	*	*	*	O/3.3	0/3.3	ON	*
(Q) Output DC volta	ge characteristics							
V ₄₃	*	*	0	0	0/3.3	0/3.3	*	*
V _{LB}	*	*	0	3.3	0/3.3	0/3.3	*	*
V _{SQ}	*	*	3.3	0	0/3.3	0/3.3	*	*

*: Any condition

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